

Fig. 1

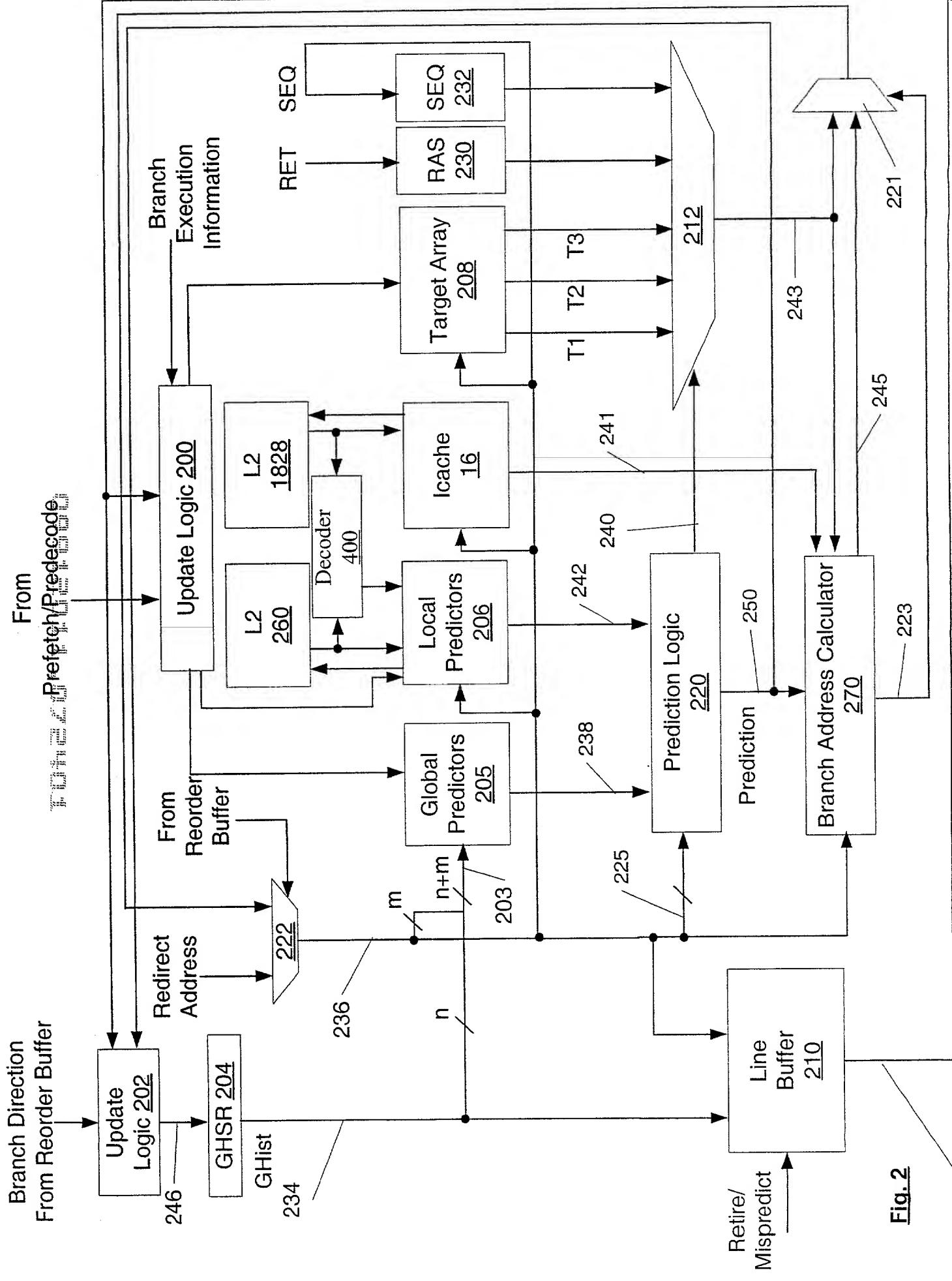


Fig. 2

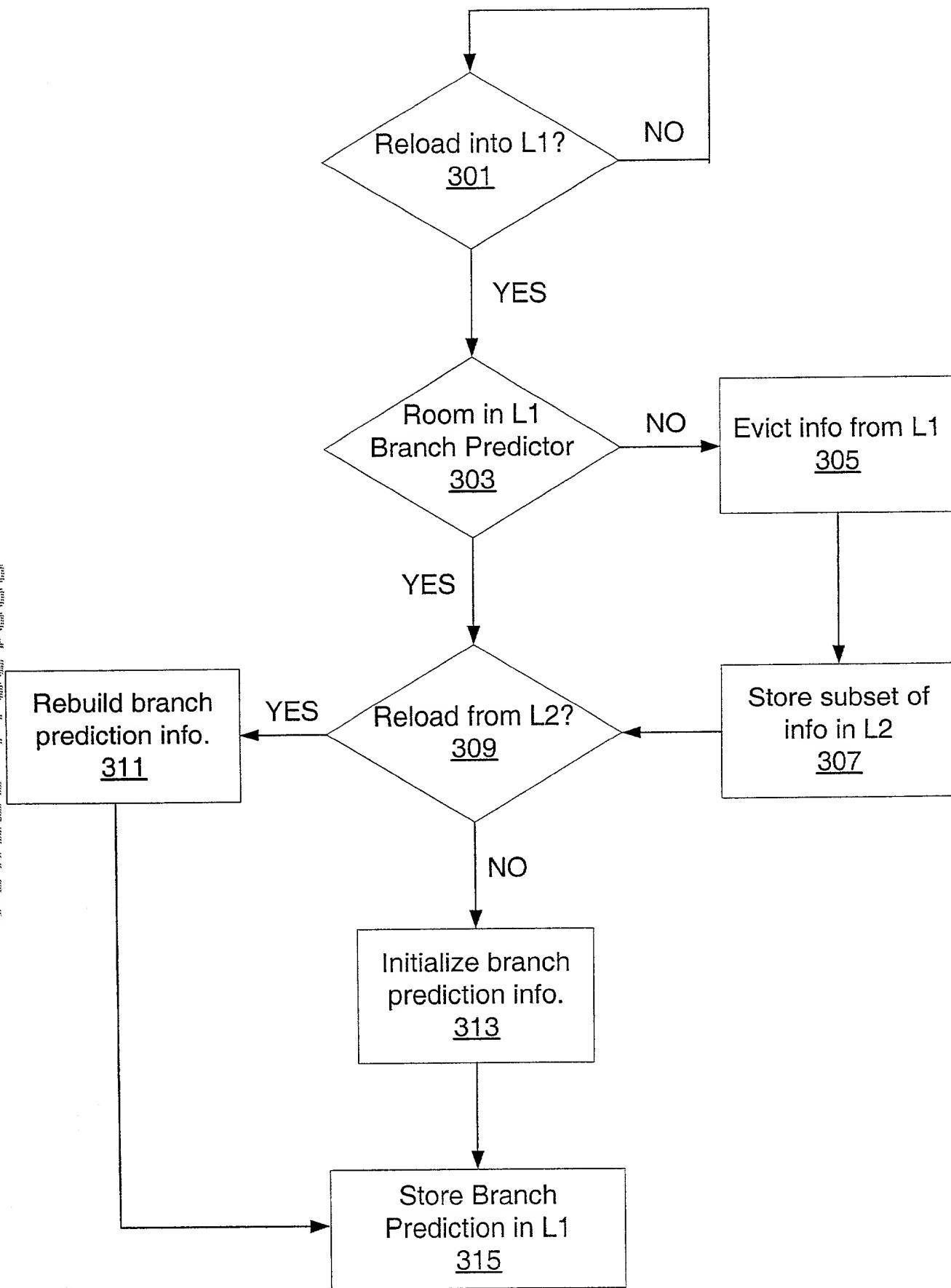


Fig. 3

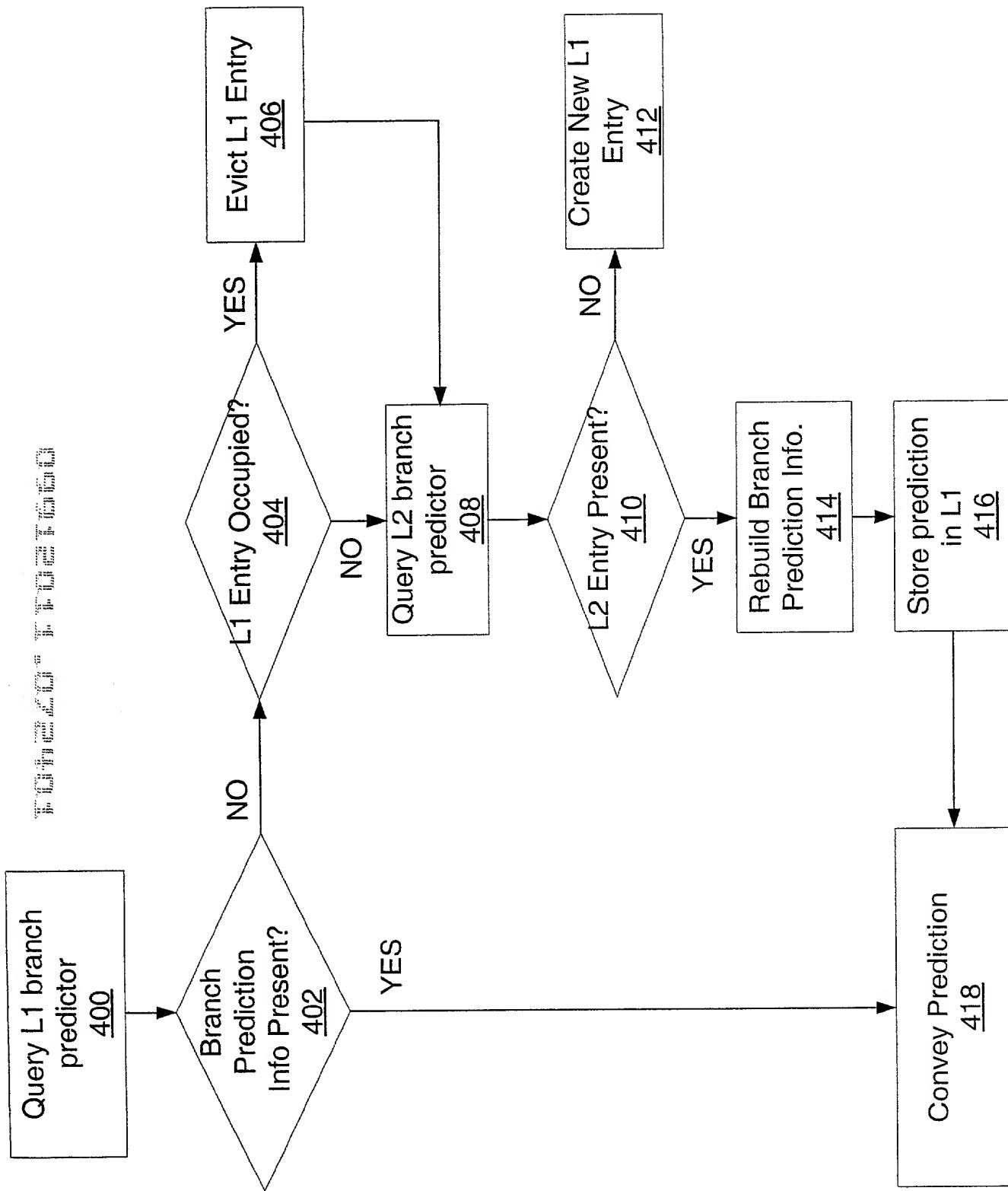


Fig. 4

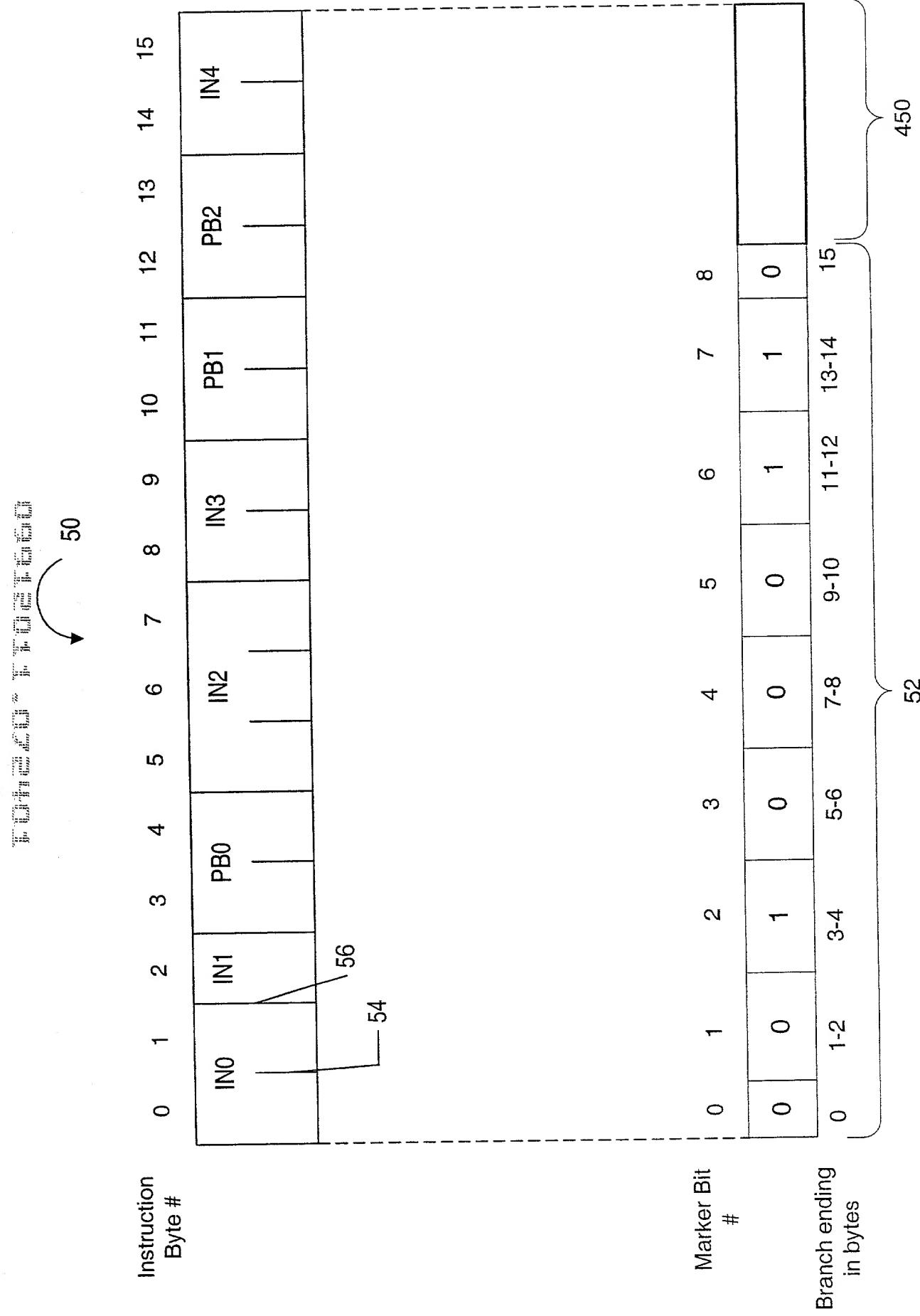


Fig.5

Offset	<=0	<=1	<=3	<=5	<=7	<=9	<=11	<=13
Marker Bit	0	1	2	3	4	5	6	7
#								8
	602	604	606	608	610	612	614	616
								618

Fig. 6

IN0 IN1 PB0 IN2 IN3 PB1 PB2 IN4

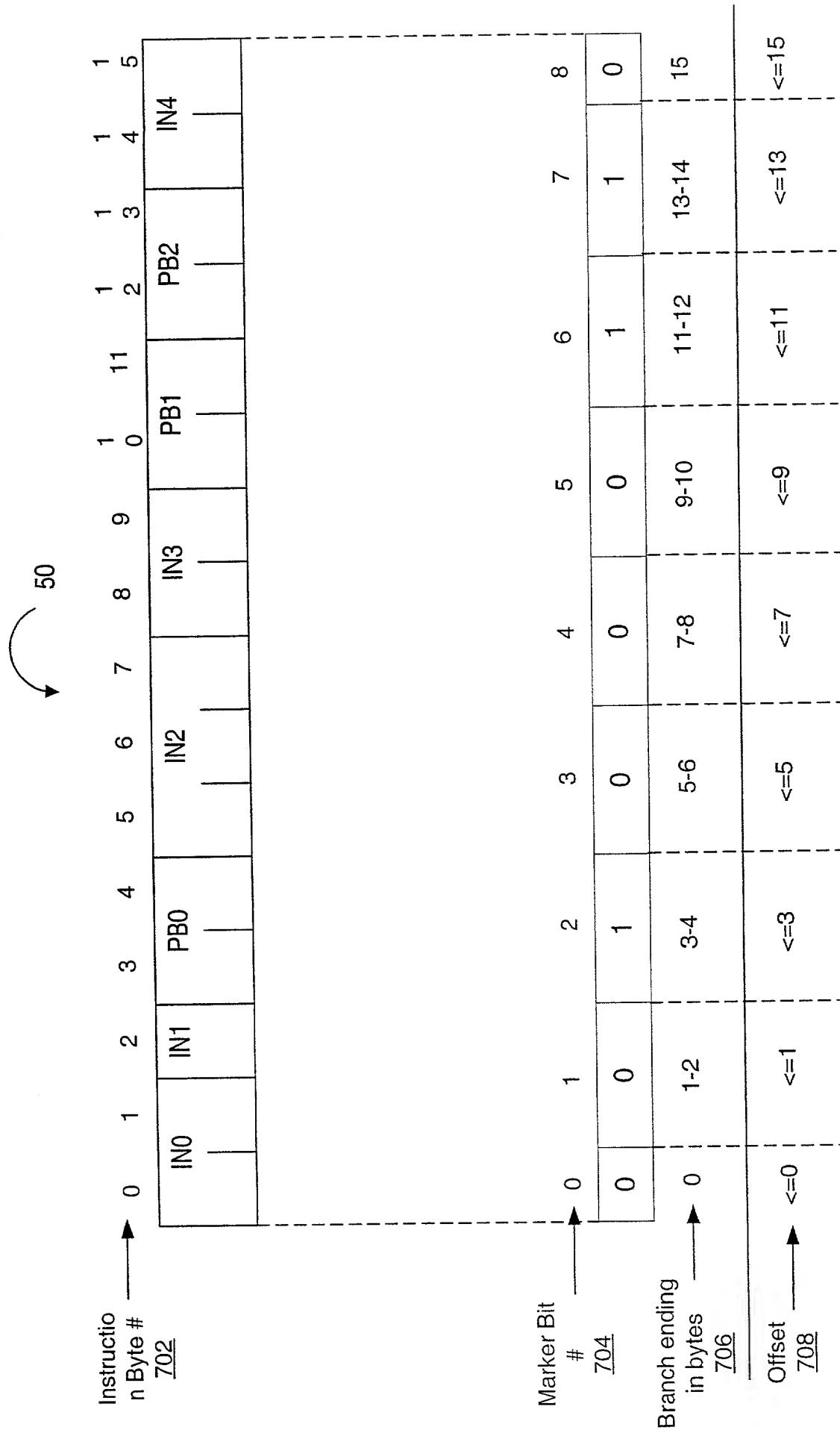


Fig. 7

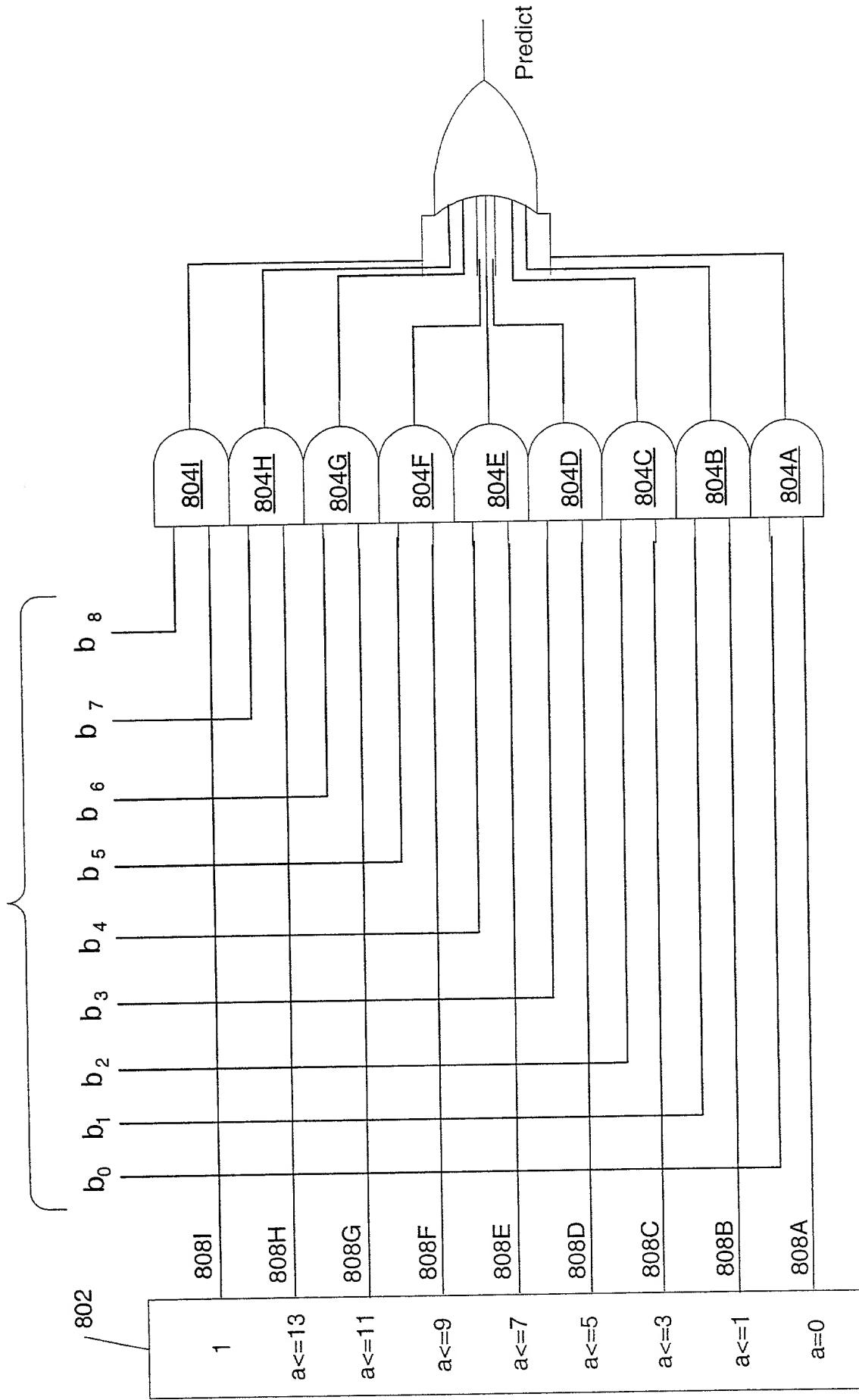


Fig. 8

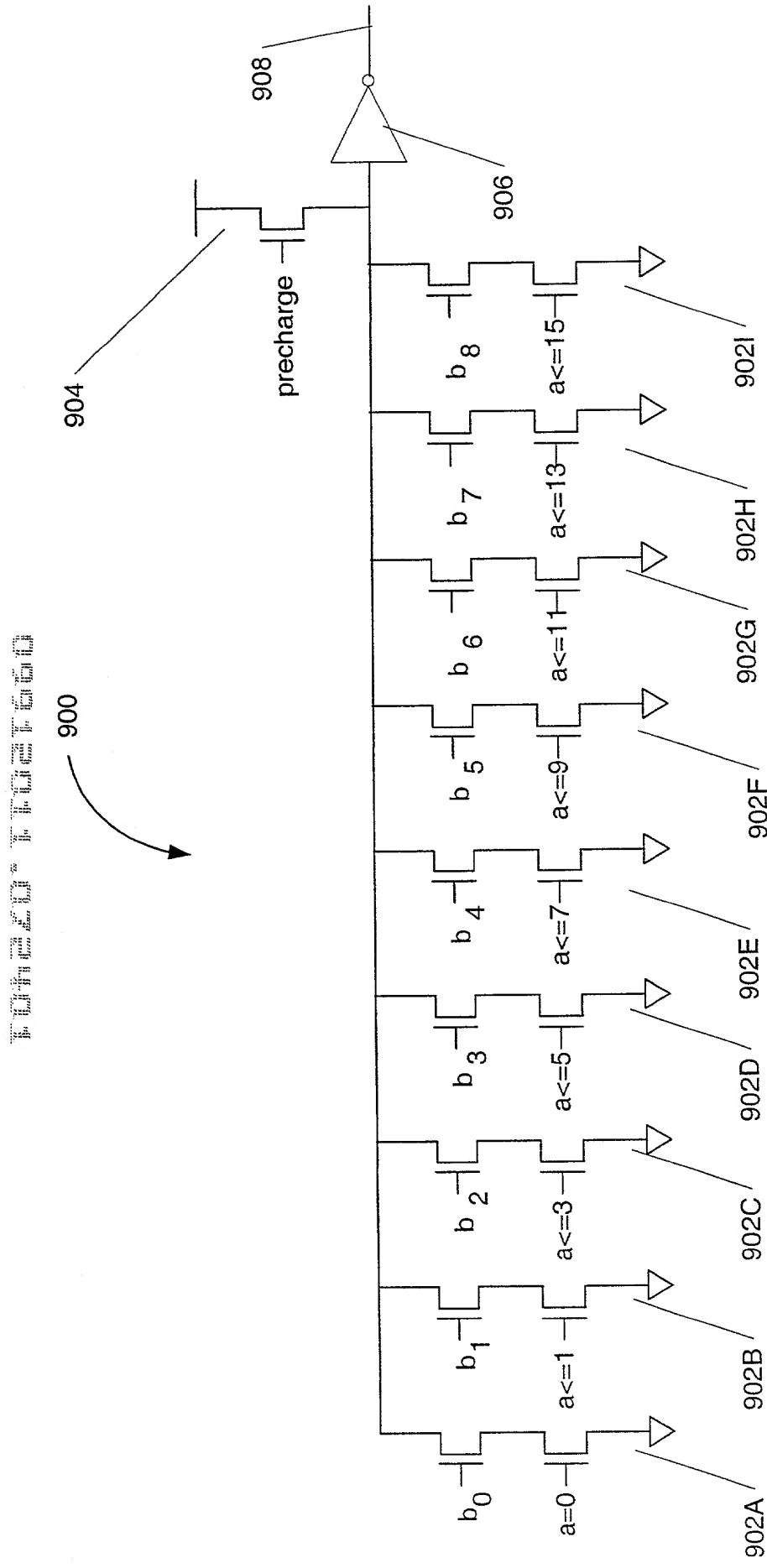


Fig. 9

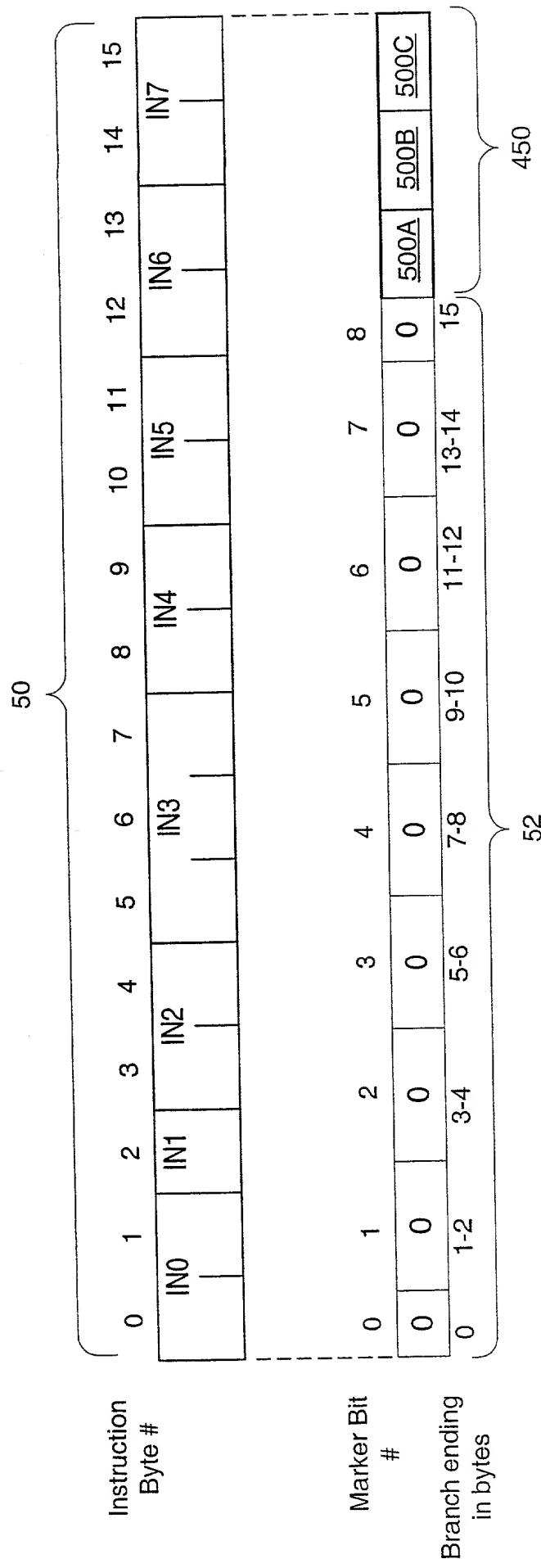


Fig. 10

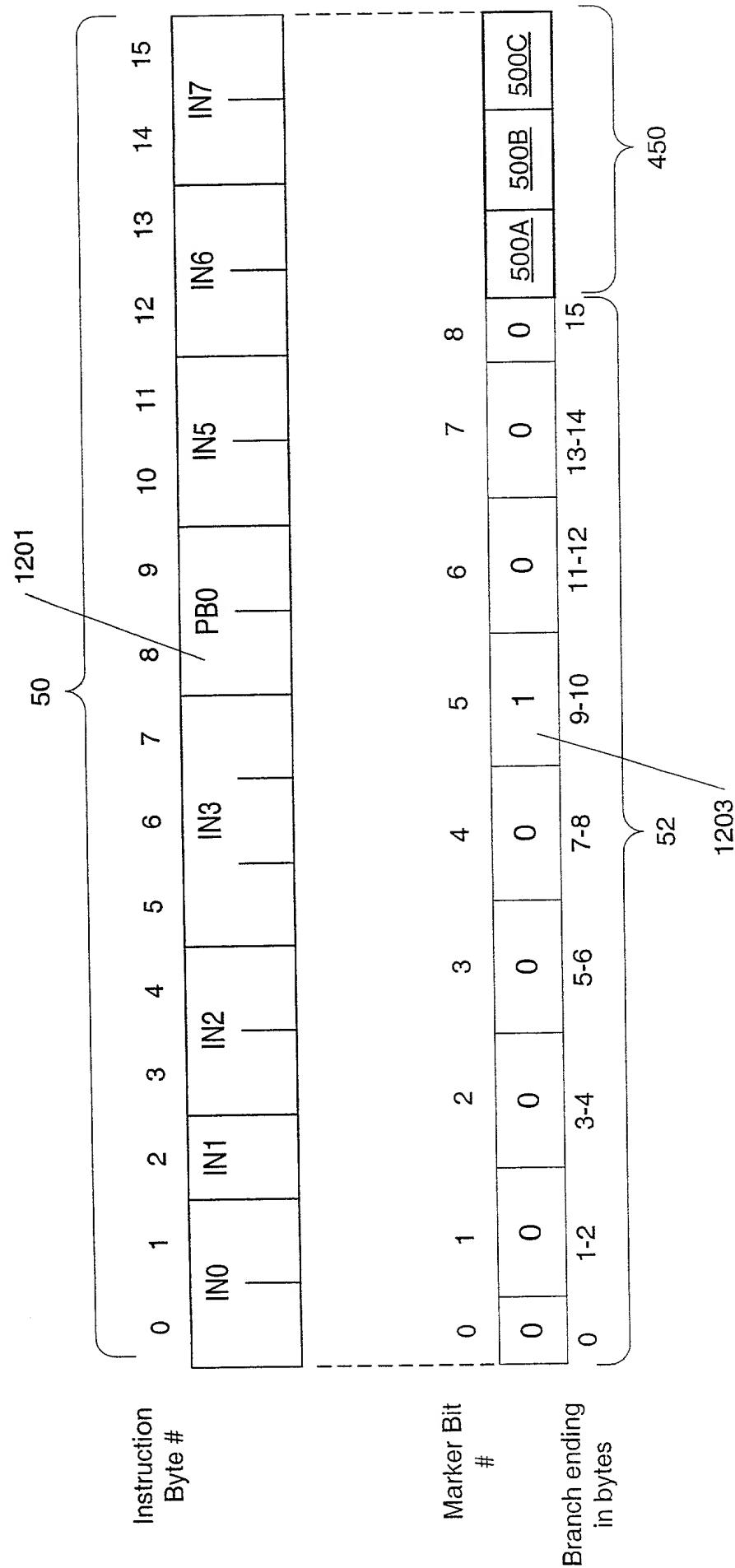


Fig. 11

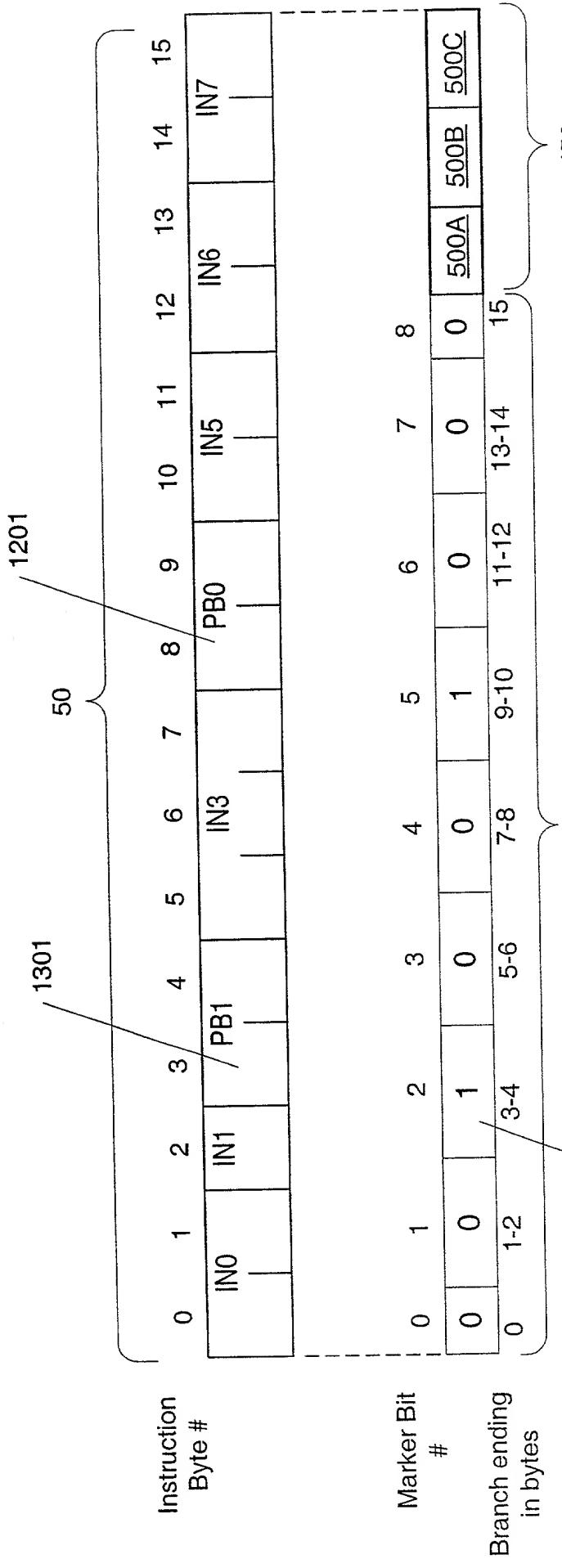


Fig. 12

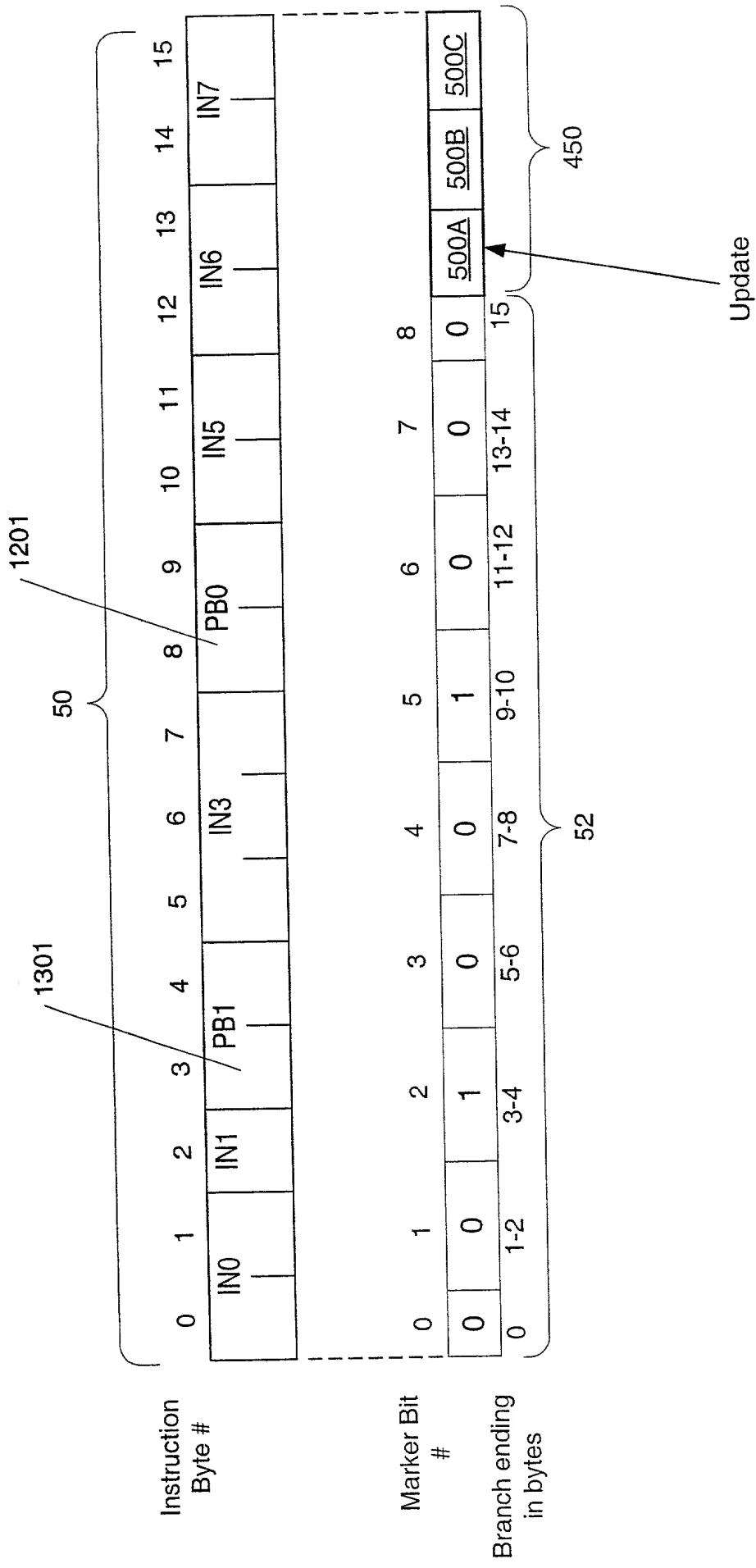


Fig. 13

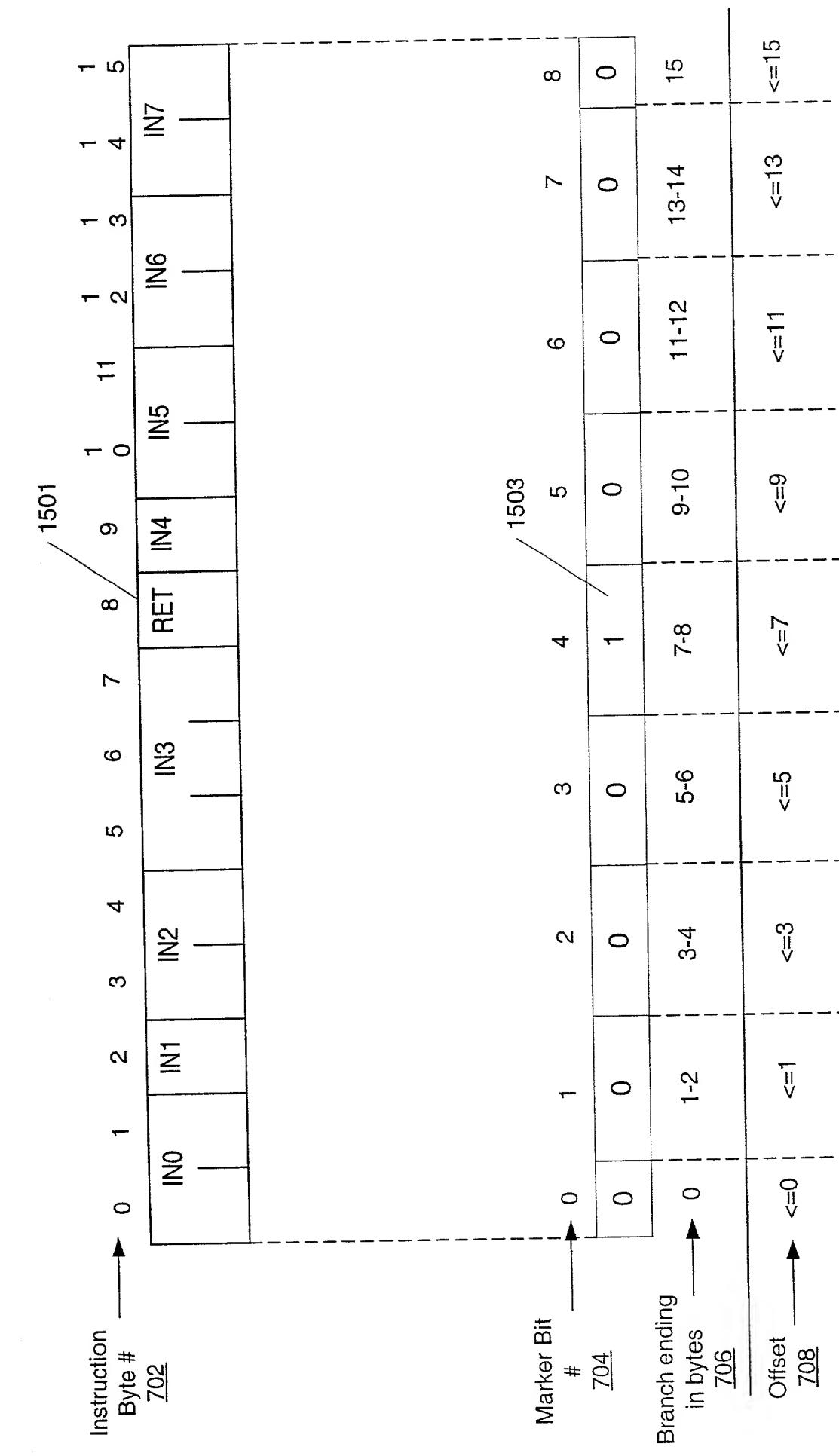
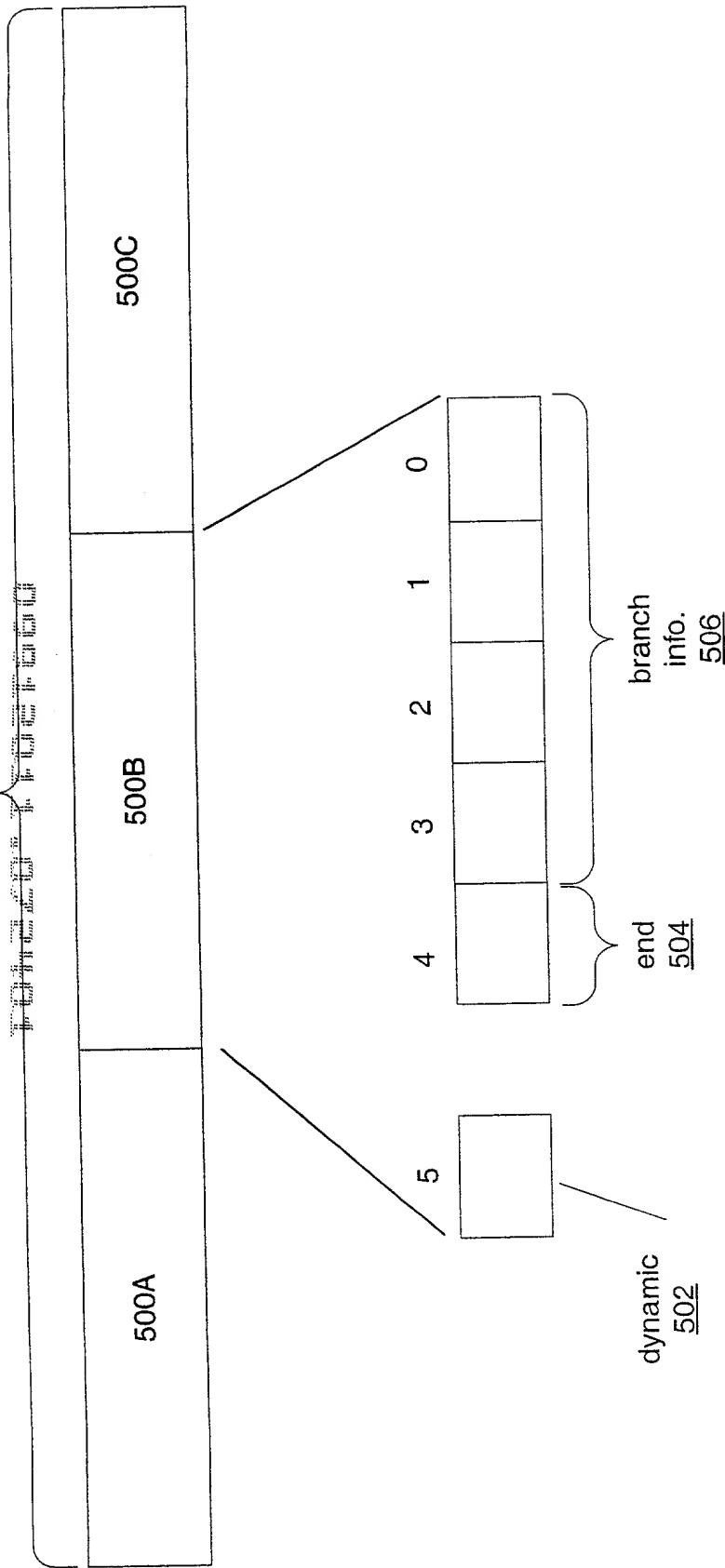


Fig. 14

450



jcc	4	3	2	1	0	508
call	end	0	0	size		510
ret	end	1	0	0	0	512
C3	end	1		even position		514

Fig. 15

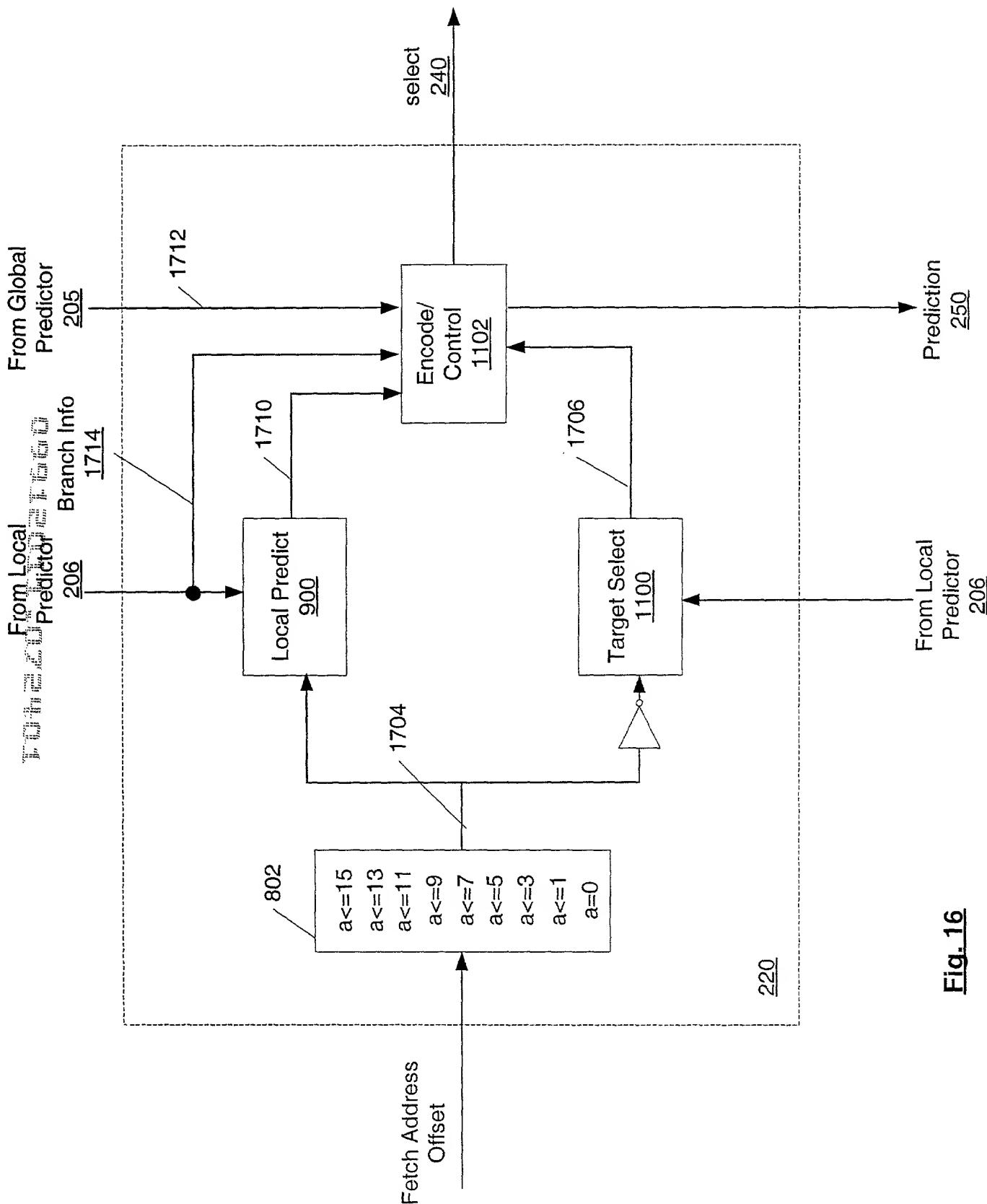


Fig. 16

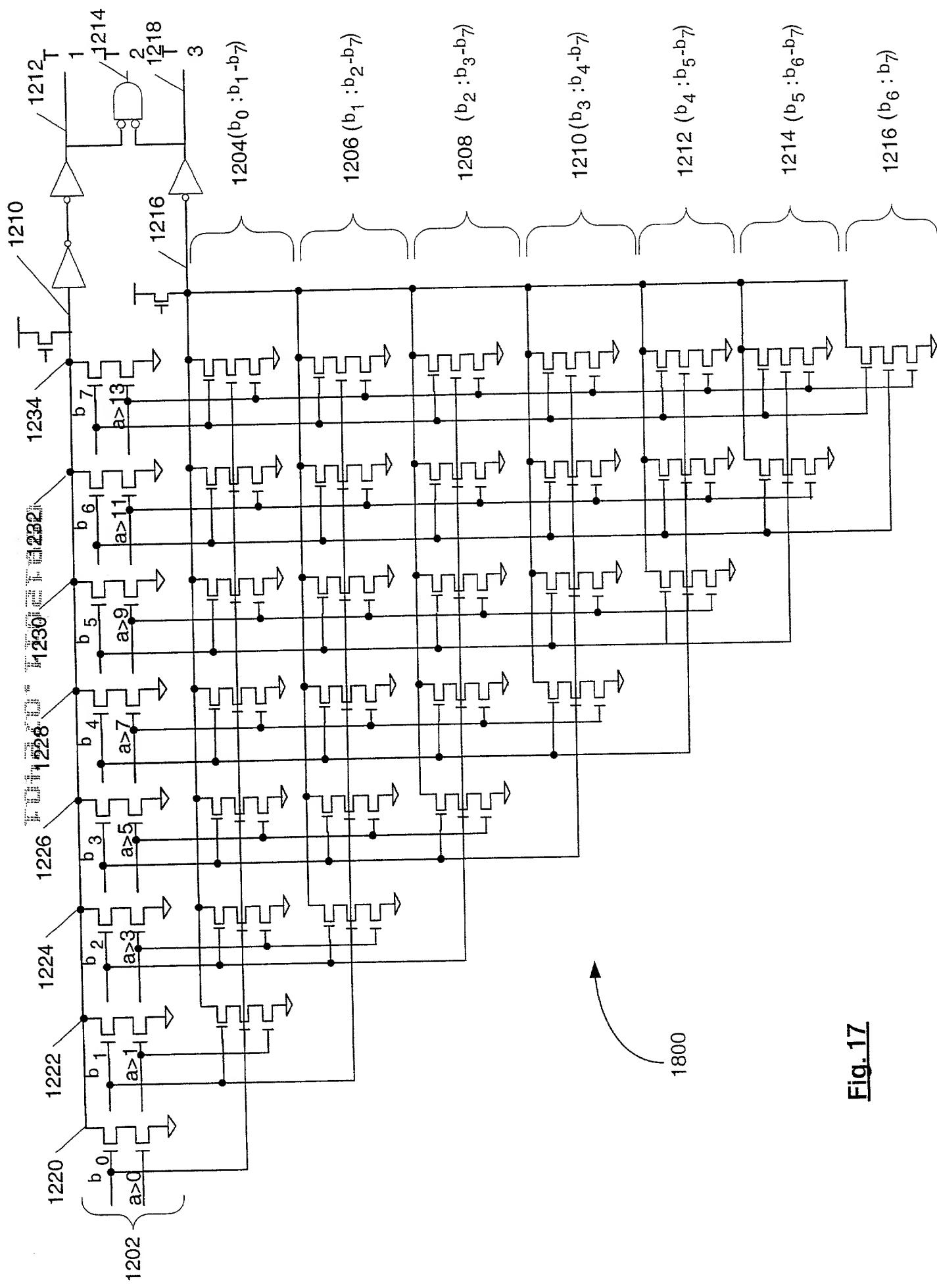


Fig. 17

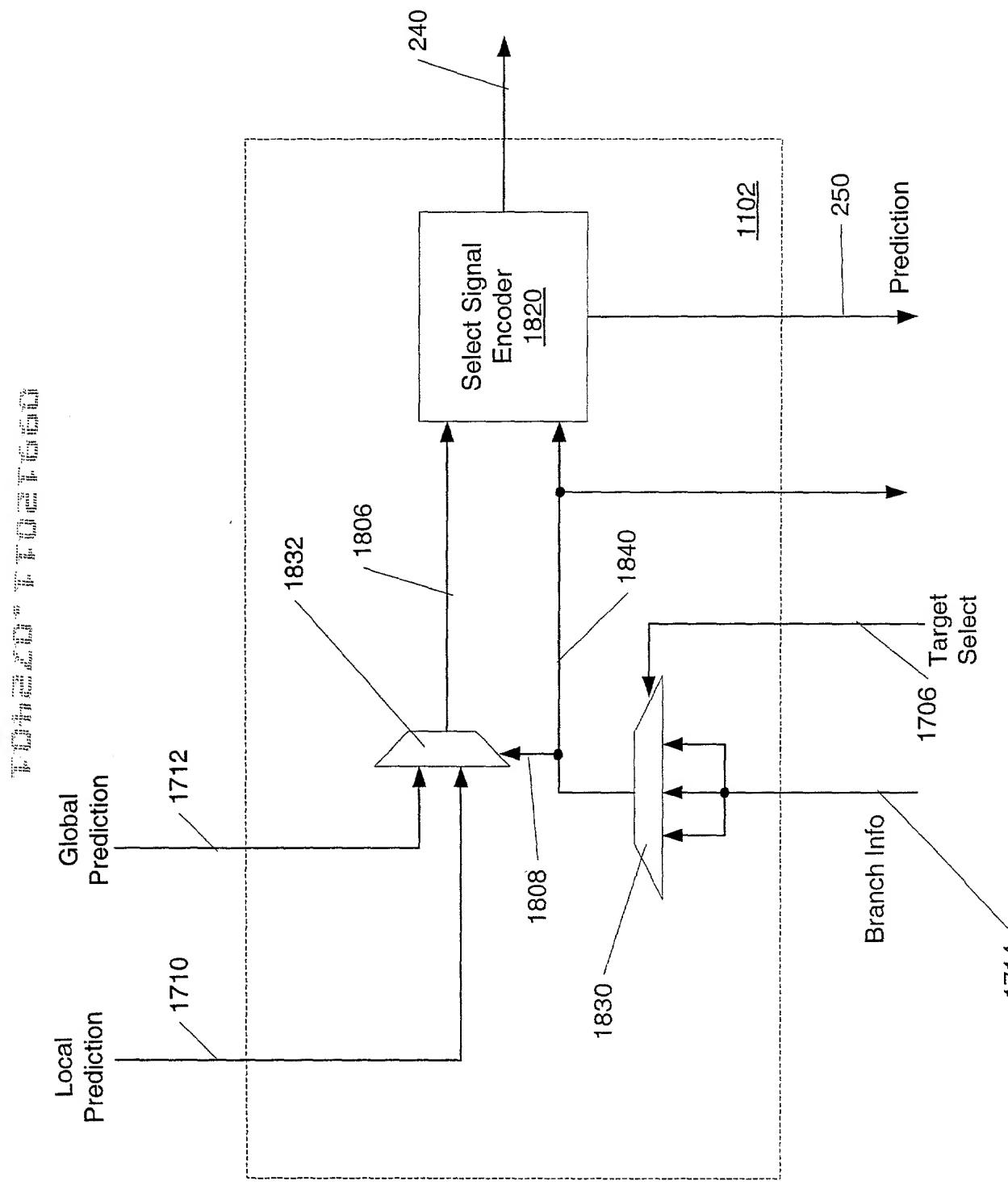


Fig. 18

From Prediction Logic 220
From Cache 160

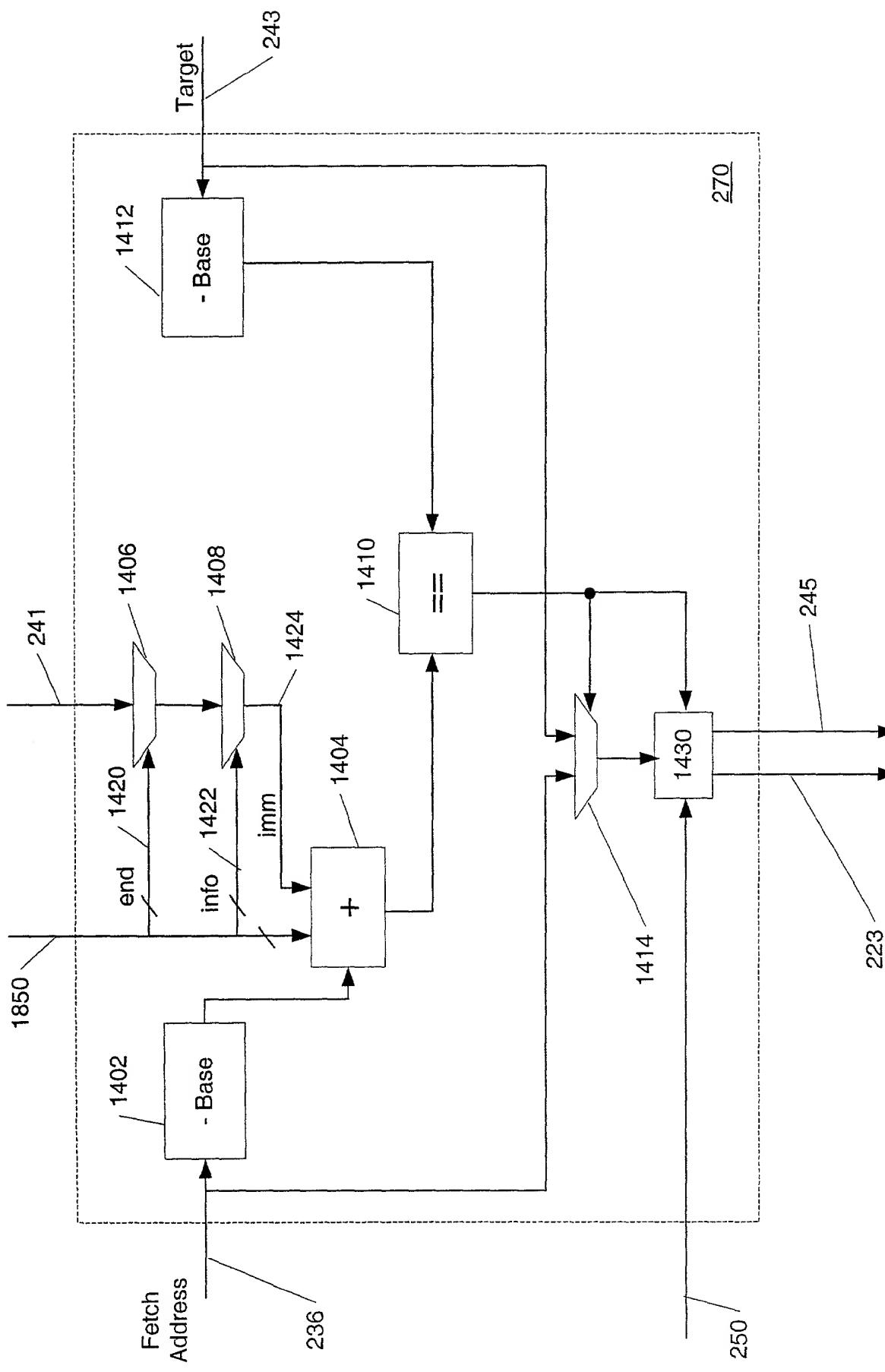


Fig.19

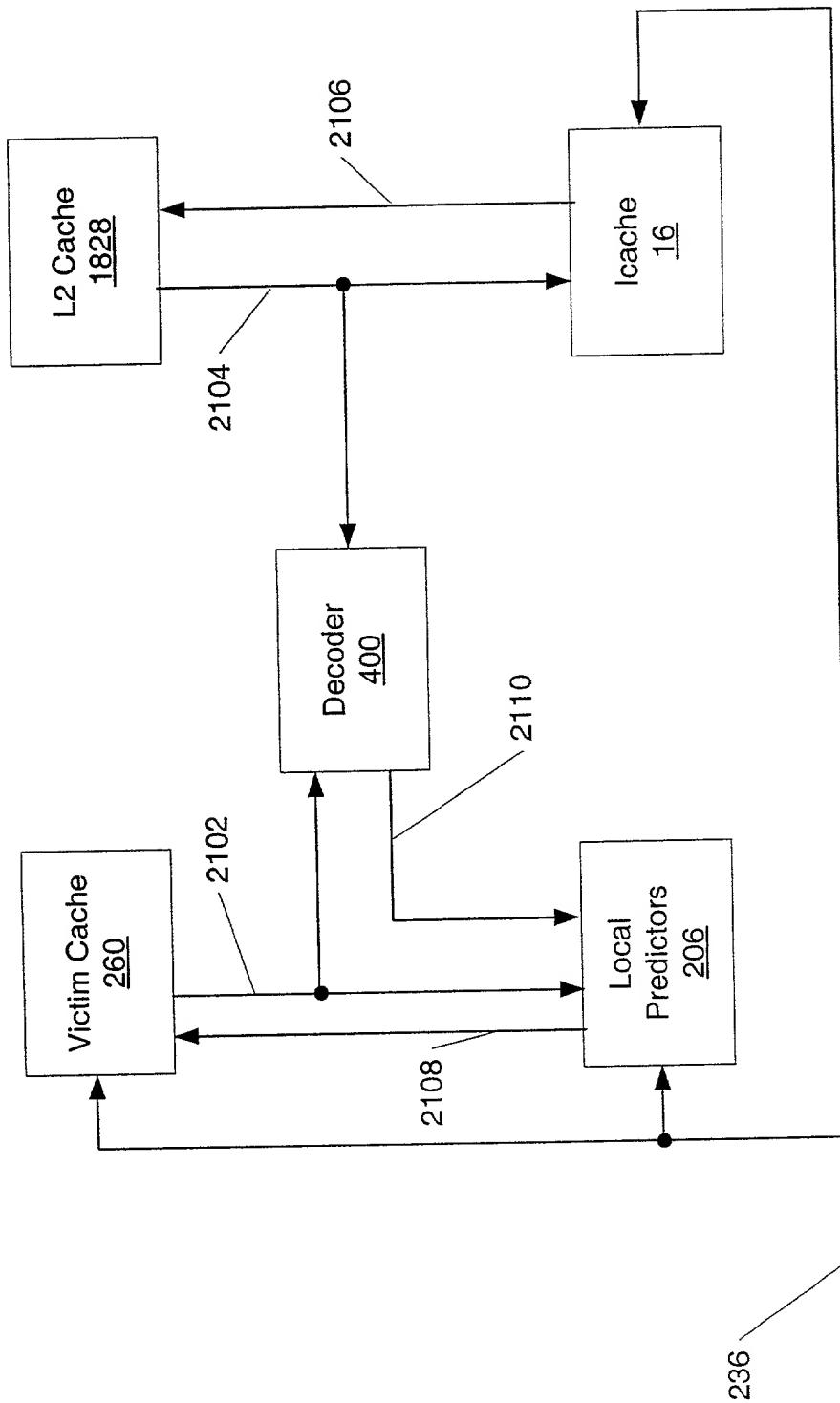


Fig. 20

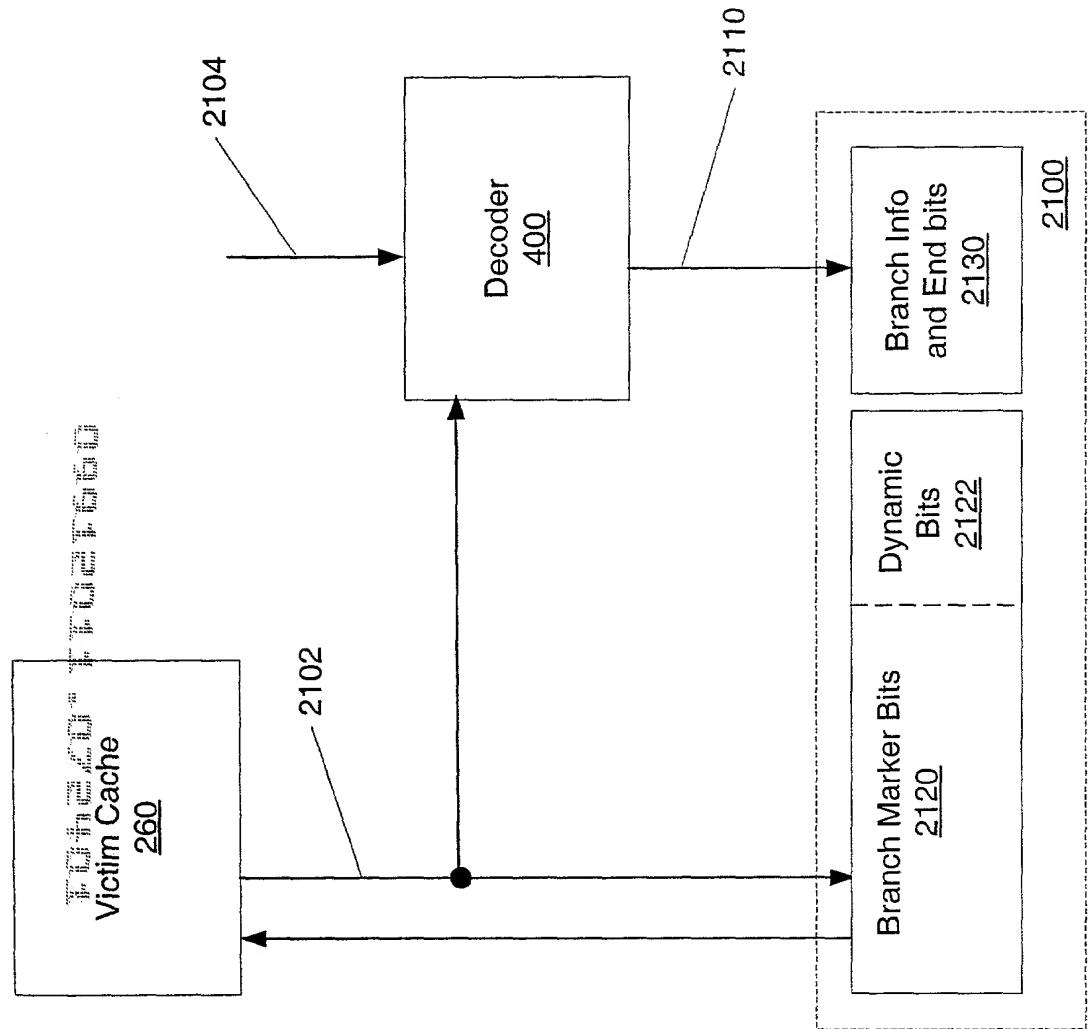


Fig.21

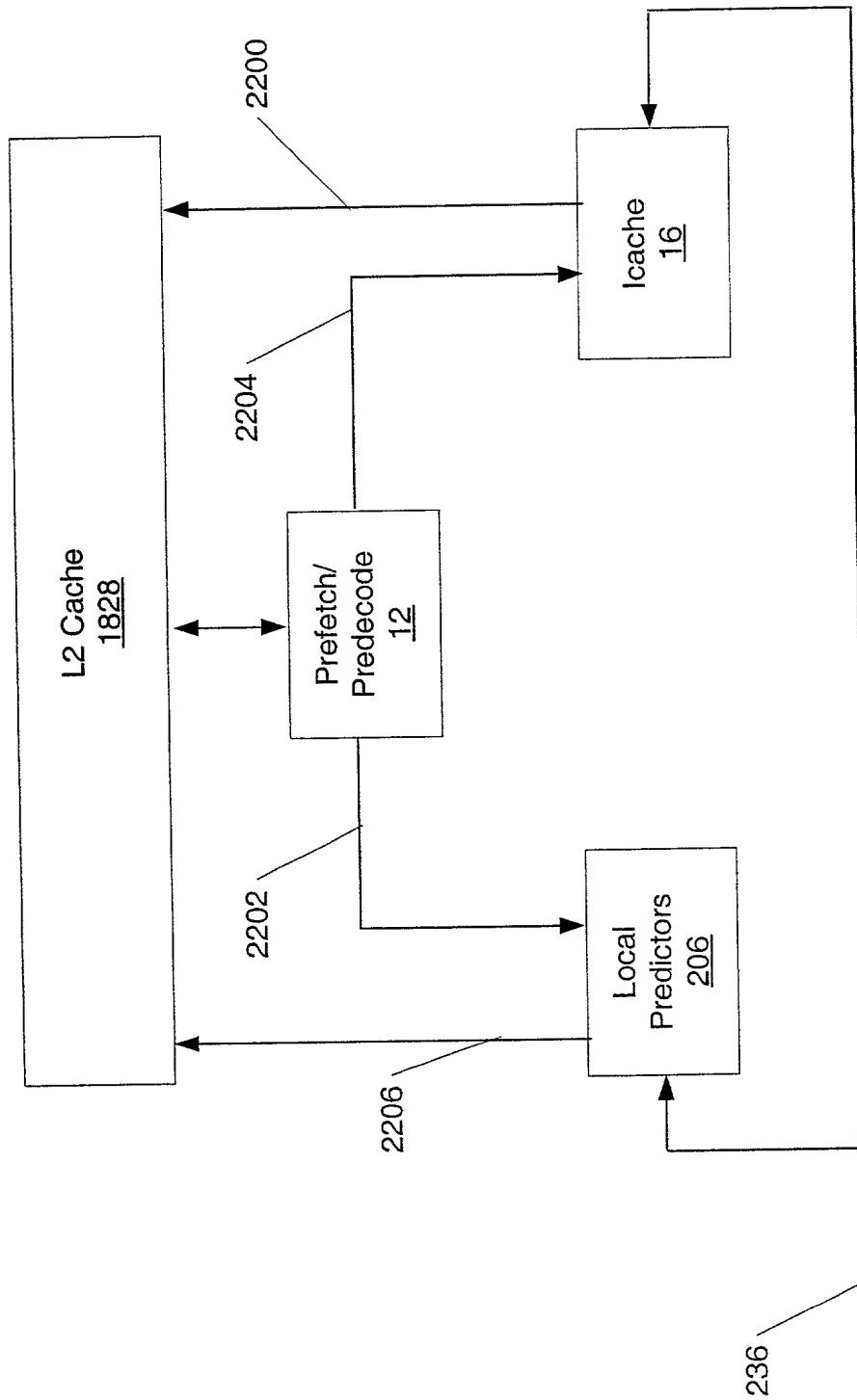


Fig. 22

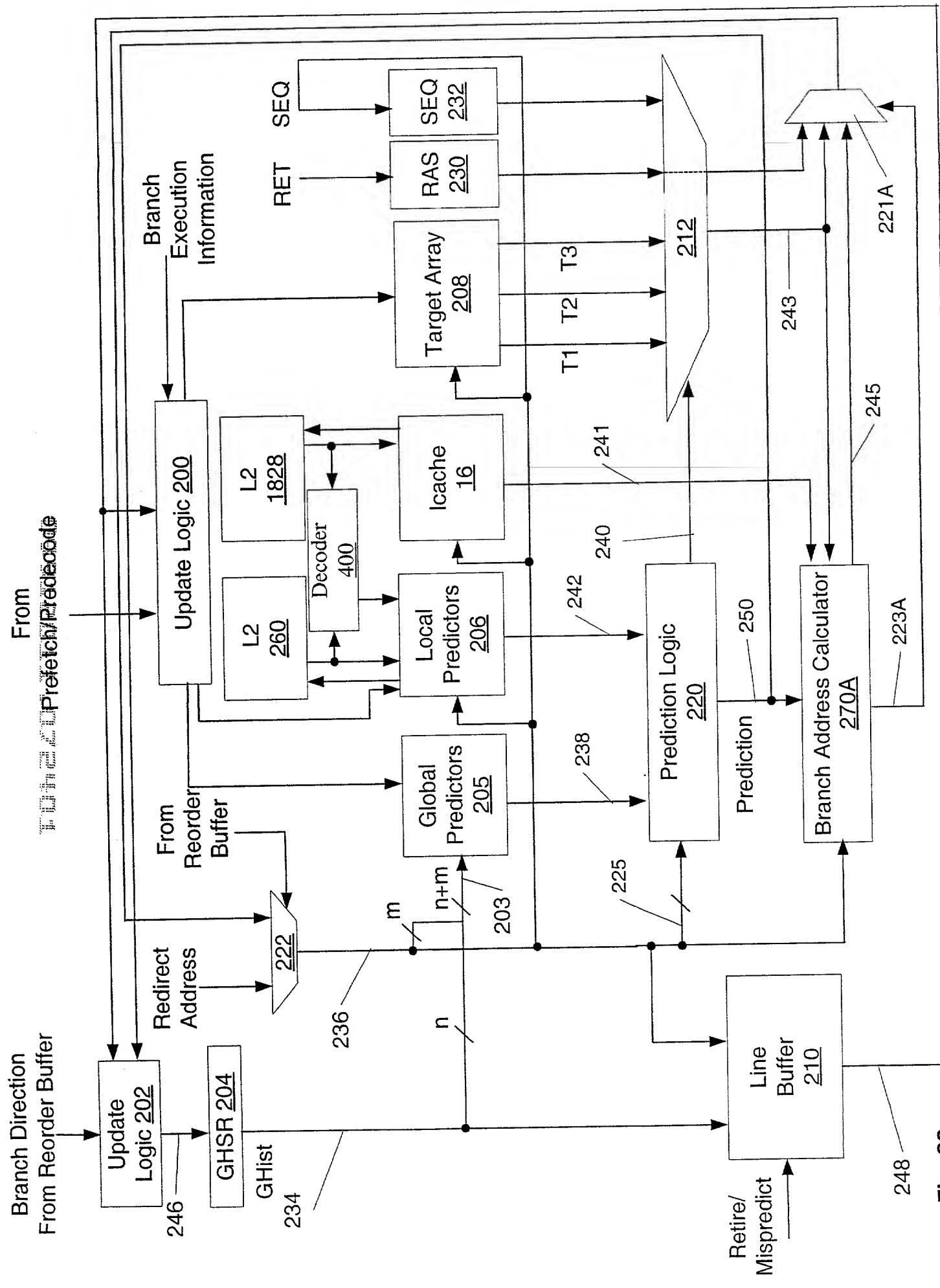


Fig. 23

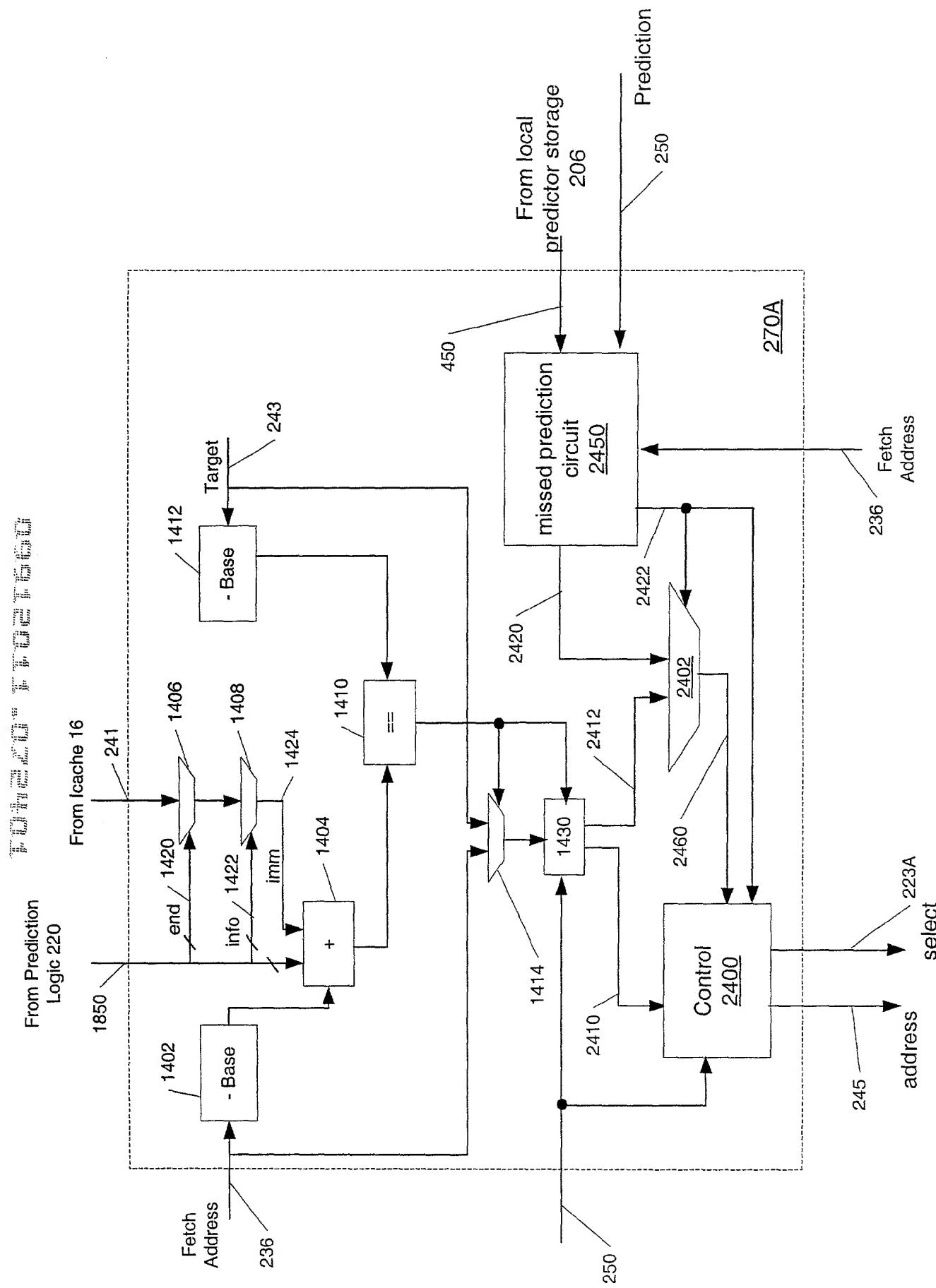


Fig. 24

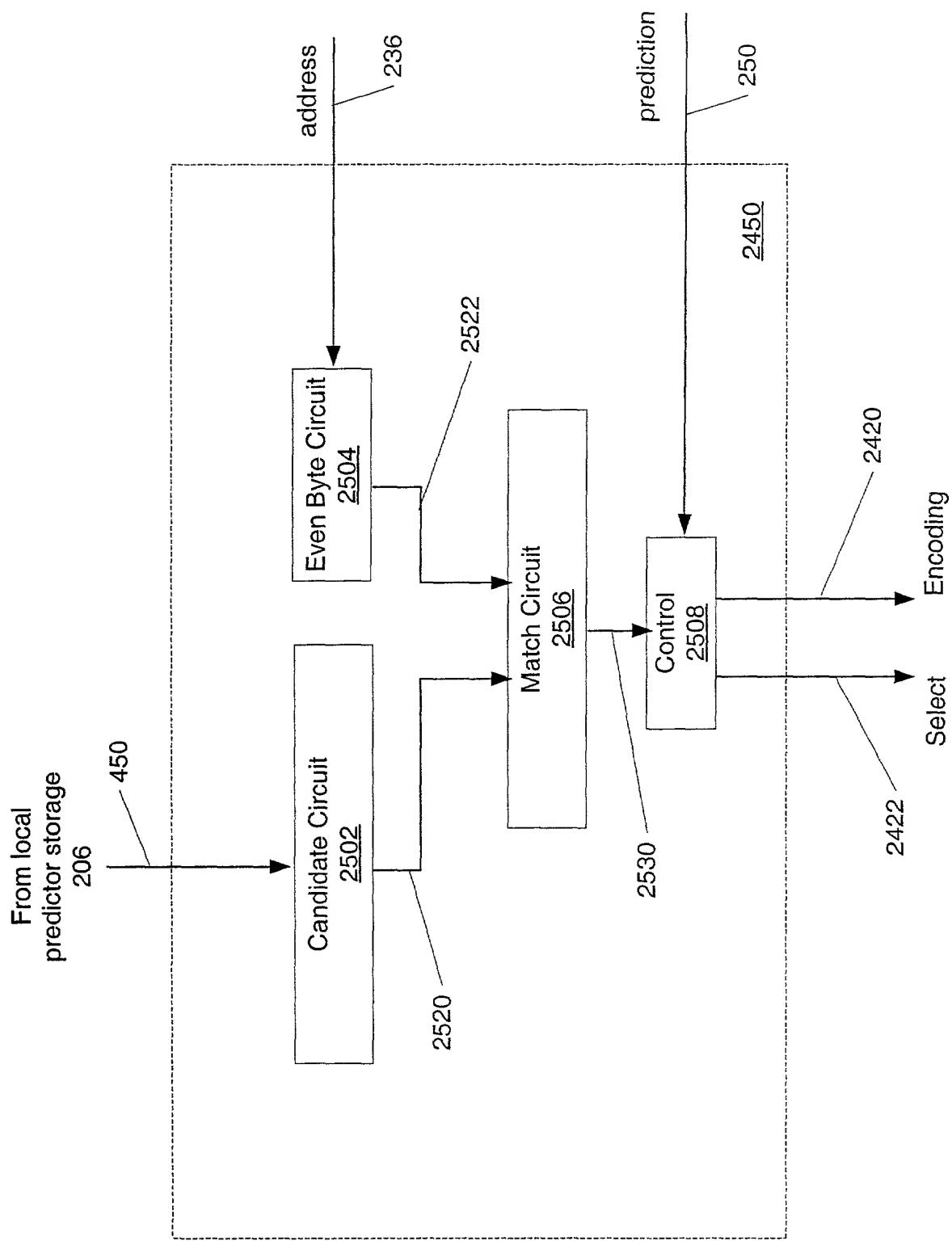


Fig. 25

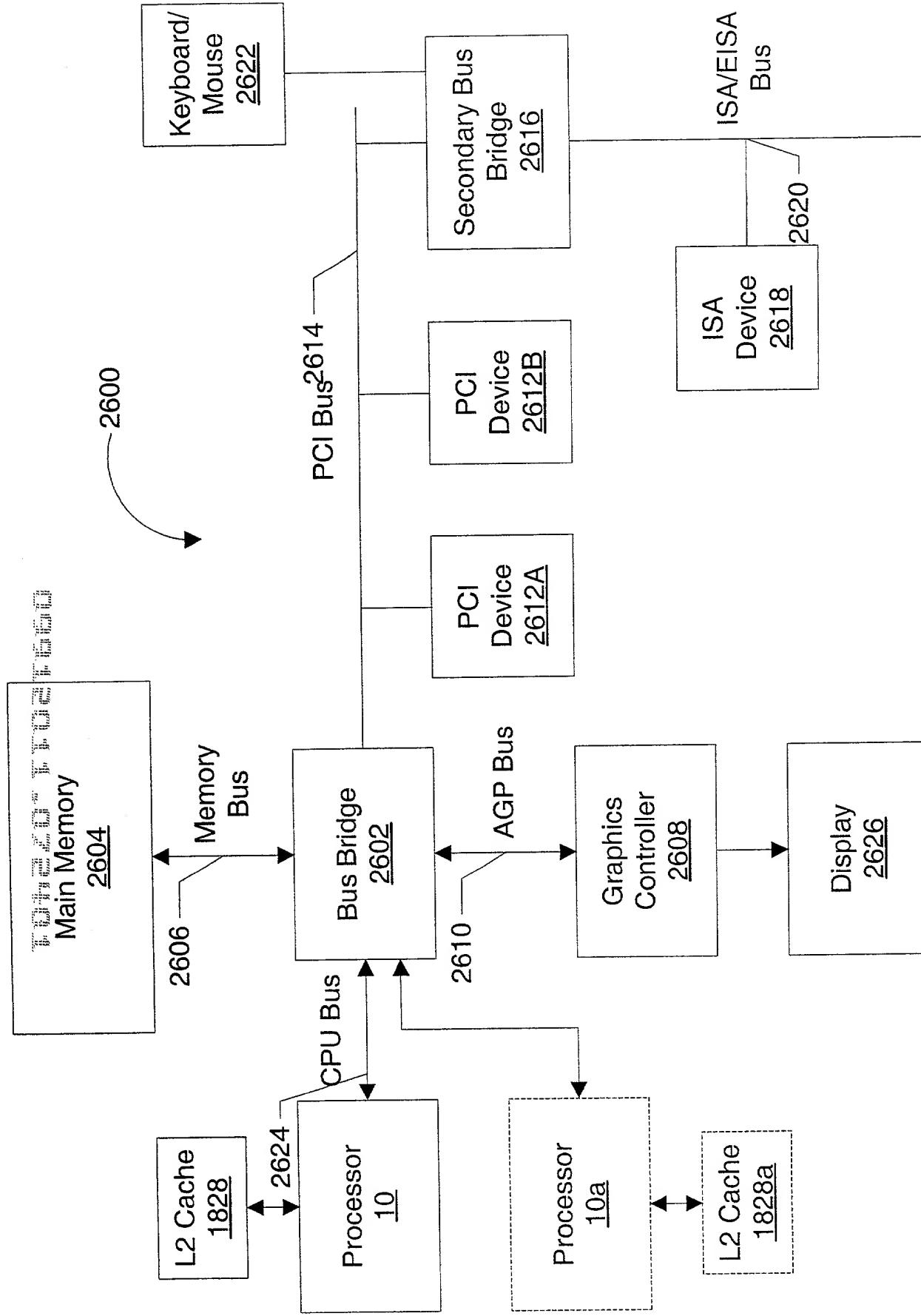


Fig. 26